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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,006	KELLAR ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,7,9,10,14,16-18 and 21 is/are rejected.

7)☒ Claim(s) 4-6,8,11-13,15,19,20 and 22 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 July 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/7/03, 9/23/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "dielectric recess" must be shown or the feature canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim requires a "dielectric recess." Since the specification only suggests that such a feature is present without describing its physical form, and since the feature is absent from the drawings, it is unclear as to exactly what form the "dielectric recess" takes, and how, exactly, it "ensures that the metallic lines deposited on the surface of one wafer are bonded with the metallic lines deposited on the surface of the other wafer."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 7, 9, 14, 16, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,724,084 to Hikita et al.

Regarding claims 1, 9, and 16, Hikita discloses a wafer bonding method having the steps of: forming a first wafer ('bottom' 80 in figures 4a, 4b) and a second wafer ('top' wafer in

figures 4a, 4b), each including one or more integrated circuit devices (column 9, line 55 – column 11, line 15), metallic lines (88) deposited via an interlevel dielectric (84, 85; figures 1A-1E), and at least one barrier line (87) deposited on an outer edge of the surface (figures 3-4); wherein the metallic lines and the barrier line deposited on the surface of the second wafer are selectively aligned to the first wafer (column 11, lines 1-24), bonded with the lines on the surface of the first wafer (figures 3, 4) to establish electrical connections between active IC devices and form a barrier structure (column 11, lines 9-15; figures 3-4).

Regarding claims 7, 14, and 21, Hikita discloses that the wafers correspond to a single die (figures 4a, 4b), and the barrier structure is formed by one line deposited on the outer edge of the bonded die (figures 4a, 4b). Since the barrier is a metal layer provided enclosing the outer periphery of the bonded dice, it inherently protects them from corrosion, contamination, and crack propagation.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 10, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. in view of U.S. Patent No. 6,340,608 to Chooi et al.

Hikita discloses bonding pads (88) deposited on opposing surfaces of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers (see column

9, line 55 – column 11, line 15; figures 1-4), and that the bond pads and barrier lines are formed of the same material (see figures 1-2).

Hikita fails to specify that the bond pads are made of copper.

Chooi teaches that copper interconnection pads for flip chip bonding are advantageous over other connection joints (see column 1, lines 5-18, column 3, lines 1-10, and column 4, lines 1-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Hikita, such that the bonding pads and barrier are formed of copper, as suggested by Chooi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use copper as a bond pad/interconnection material, because Chooi shows that it has low inductance, low capacitance, lower cost, and simpler fabrication processes than conventional flip chip bonding pads (Chooi, column 1, lines 5-18; column 3, lines 1-10; column 4, lines 1-13).

Allowable Subject Matter

8. Claims 4-6, 8, 11-13, 15, 19, 20, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 4-6, 11-13, 19, and 20, the primary reason for allowability is that the prior art only teaches the usage of a barrier structure as claimed for a single die, and hence, does not suggest applying a barrier to an outer edge of a bonded wafer having a plurality of dice. Since

the prior art of record specifically applies such a barrier to each individual die for either hermetic sealing or stress management of that die, and since a structure having a barrier at the edge of a multi-die wafer does not provide individual sealing for each die, it is the examiner's opinion that the prior art generally teaches away from the claimed feature.

Regarding claims 8, 15, and 22, the prior art generally teaches the usage of a single guard ring deposited on the perimeter of the die, but there is no suggestion or motivation for providing a barrier in the shape of concentric rings. It is the examiner's opinion that a person having ordinary skill in the art would have simply used the single barrier ring taught by the prior art, rather than concentric rings, because the structure is simpler to fabricate.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,238,951 to Caillat, U.S. Patent No. 6,373,130 to Salaville, and U.S. Patent No. 6,643,920 to Hori disclose a method of bonding a die to a wiring substrate, wherein a peripheral barrier is used to hermetically seal and protect the die.

b. U.S. Patent No. 5,401,672 to Kurtz discloses a stacked chip structure having a peripheral sealing structure and connection portions between ICs on different substrates.

c. U.S. Patent No. 6,297,072 to Tilmans et al. discloses a chip bonded to a substrate with a sealing barrier provided at the periphery.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

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